

COMPUTER SYSTEM WITH BACKUP MANAGEMENT  
FOR HANDLING EMBEDDED PROCESSOR FAILURE

Field Of The Invention

**[0001]** The present invention relates generally to computer systems, and more particularly, to a system comprising a backup management processor that provides basic system control functions upon failure of one or more system management processors.

BACKGROUND OF THE INVENTION

Statement Of The Problem

**[0002]** Certain existing computer systems include a management processor to monitor and control aspects of the system environment such as power, power sequencing, temperature, and to update panel indicators. Failure of the management processor may result in system failure due to the inability to monitor and control system status, power, temperature, and the like.

**[0003]** Even in systems having a peer or backup management processor, however, a firmware bug common to all management processors can cause the system processor to effectively become non-operational, since all of these processors are typically programmed with essentially the same code, and thus all of them are likely to succumb to the same problem when a faulty code sequence is executed.

Solution To The Problem

**[0004]** The present system solves the above problems and achieves an advance on the field by providing a high-availability controller that monitors the status of the management processor. If the management processor should fail, the controller provides at least a minimal set of functions required to allow the system to continue to operate reliably. Furthermore, the high-availability controller does not perform the same sequence of operations as the code executed by the management processor, and therefore is not susceptible to failure resulting from a specific 'bug' that may cause the management processor to fail.

**[0005]** The present system includes a power management subsystem that controls power to all system entities and provides protection for system hardware from power and

environmental faults. The power management subsystem also controls front panel LEDs and provides bulk power on/off control via a power switch.

**[0006]** During normal system operation, the management processor monitors system sensors that detect system power, temperature, and cooling fan status, and makes necessary adjustments or reports problems. The management processor also updates various indicators and monitors user-initiated events such as turning power on or off.

**[0007]** The management processor normally provides an output signal indicating that it is operating properly. The high-availability controller monitors this signal to verify that the management processor is operating. When the management processor indicates that it is not operating properly, the high-availability controller monitors the system sensors and updates system indicators. If a problem develops, such as failure of a power supply or a potentially dangerous increase in temperature, the high-availability controller powers down the appropriate equipment to protect the system from damage. In addition, if a system user decides to power down the system, the high-availability controller is responsive to the power switch, which can be used to initiate powering down of the system when the management processor has failed.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0008]** Figure 1 is a block diagram illustrating basic components of the present system;

**[0009]** Figure 2 is a block diagram illustrating exemplary components utilized in one embodiment of the present system;

**[0010]** Figure 3 is a flowchart showing an exemplary sequence of steps performed by the high-availability controller in accordance with the present system;

**[0011]** Figure 4 is a block diagram illustrating, in greater detail, components of the high-availability controller of the present system; and

**[0012]** Figure 5 is a flowchart showing an exemplary sequence of steps performed by the high-availability controller operation state machine.

## DETAILED DESCRIPTION

**[0013]** Figure 1 is a block diagram illustrating basic components of the present system 100. As shown in Figure 1, the high level components of system 100 comprise one or more management processors 105, a high-availability controller 101, power, fan, and system

temperature sensors 120, front panel indicators 130, cooling fan controller module 140, a plurality of power controllers 150, and a power switch 110.

**[0014]** Management processor 105 monitors and controls various aspects of the system environment such as power, via power controllers 15x (local power modules 151, 152, and 153, shown in Figure 2); temperature, via cooling fans controlled by module 140; and updating panel indicators 130. Management processor 105 manages operations associated with core I/O board 104, which includes I/O controllers for peripheral devices, bus management, and the like. High-availability controller 101 monitors the status of management processor 105, and as well as power, fan, and temperature sensors 120. In the situation wherein high-availability controller 101 detects failure of the management processor 105, it assumes control of the system 100, as described below in greater detail.

**[0015]** Since the high-availability controller does not perform the same sequence of operations as the code executed by the management processor, it is therefore not susceptible to failure resulting from a specific ‘bug’ that may cause the management processor to fail.

#### Normal System Operation

**[0016]** While management processor 105 is operating properly, the following events take place. When the front panel power switch 110 is pressed, high-availability controller 101 recognizes this and notifies the management processor via an interrupt. The management processor evaluates the power requirements versus the available power and, if at least one system power supply is available and working properly, management processor 105 commands the high-availability controller to power up the system.

**[0017]** Figure 2 shows components utilized in an exemplary embodiment of the present system in greater detail. During normal system operation, when front panel power switch 110 is pressed, the following components are powered up:

- (1) system backplane 118;
- (2) PCI (I/O card) backplane 125; and
- (3) associated cell board 102.

**[0018]** Note that system 100 may include a plurality of PCI backplanes 125, each of which may contain a plurality of associated cell boards 102. In the present system, a cell (board) 102 comprises a plurality of processors 115 and associated hardware/firmware and memory (not shown); a local power module 152 for controlling power to the cell; and a local service processor 116 for managing information flow between processors 115 and external entities including management processor 105.

**[0019]** The front panel power switch 110 controls power to system 100 in both hard- and soft-switched modes. This allows the system to be powered up and down in the absence of a management processor 105. When front panel power switch 110 is pressed, if no cell board 102 is present, its PCI backplane 125 is not powered up; if a cell board is present, but no PCI backplane is present, the cell board is powered up, nevertheless. When the front panel power switch is again pressed, management processor 105 is again notified by an interrupt. Management processor 105 then notifies the appropriate system entities and the system is powered down.

**[0020]** A Cell\_Present signal 114 is routed to the system board (and to high-availability controller 101) through pins located on the connector on the cell board 102. If the cell board is unplugged from the system board, the Cell\_Present signal 114 is interrupted causing it to go inactive. High-availability controller 101 monitors the Cell\_Present signal and, if a Cell Power Enable signal 113 is active to a cell board 102 whose 'Cell Present' signal 114 goes inactive, the power to the board is immediately disabled and stays disabled until the power is explicitly re-enabled to the cell board. A 'Core IO Present' signal 109 is routed to the system board through pins located on the core I/O board connector. If the core I/O board 104 is unplugged, the Core IO Present signal 109 is interrupted, causing it to go inactive.

**[0021]** Core I/O board 104 includes a watchdog timer 117 that monitors the responsiveness of management processor 105 to aid in determining whether the processor is operating properly. Management processor 105 includes a firmware task for checking the integrity of the system operating environment, thus providing an additional measure of proper operability of the management processor.

#### Operation without a Management Processor

**[0022]** Figure 3 is a flowchart showing an exemplary sequence of steps performed in practicing a method in accordance with the present system. Operation of the system may be better understood by viewing Figures 2 and 3 in conjunction with one another. In an exemplary embodiment of the present system, the operations described in figure 3 are performed by operation state machine 103. As shown in Figure 3, at step 300, high-availability controller state machine 103 monitors the status of management processor 105 via 'management processor OK' (operational) [MP\_OK] signal 108. At step 305, if MP\_OK signal 108 is detected as active, management processor 105 is assumed to be operating properly, and state machine 103 continues the monitoring process, at step 300.

[0023] If state machine 103 detects MP\_OK signal 108 as not active, the HAC assumes that management processor 105 is either not present in the system or not operational, and takes over management of system 100, at step 310, with the system in the same operational state as existed immediately prior to failure of management processor 105.

[0024] High-availability controller 101 enables the system and I/O fans 145 via fan controller module 140. Fan module 140 recognizes that a management processor is not operational, via an inactive SP\_OK (management processor OK) signal 141 from HAC 101, and sets its fan speed to an appropriate default for unmonitored operation. Should a fan fault be detected by fan module 140, high-availability controller 101 recognizes this (via a fan fault interrupt from the fan module) and powers down the system.

[0025] The 'Cell Present' signal 114 is routed to high-availability controller 101 through pins located on the cell board connector. If the cell board is unplugged, the Cell Present signal is interrupted, causing it to go inactive. State machine 103 monitors the Cell Present signal 114, and, if Cell Power Enable 113 is active to a cell board whose Cell Present signal 114 goes inactive, the power to the board is immediately disabled and will stay disabled until the power is explicitly re-enabled to the board. The Core IO Present signal 109 is routed to the HAC through pins on the core I/O board connector. If the core IO board 104 is unplugged, the Core IO Present signal 109 is interrupted, causing it to go inactive.

[0026] The following basic signals, provided by each powerable entity (cell(s) 102, system backplane 118, and PCI backplane 125), are used by the high-availability controller (HAC) 101:

- (1) a 'power enable' signal (113, 122) from the 101 (HAC) to the entity LPM;
- (2) a 'device present' signal (109, 114) to the HAC;
- (3) a 'device ready' signal to HAC;
- (4) a 'power good' signal to the HAC; and
- (5) a 'power fault' signal to the HAC (except for cell LPM fault indications, which are provided to the local service processor 116 for the cell). For the sake of clarity, each of the latter three signals [(3)–(5)] is combined into a single line in Figure 2, as shown by lines 112, 119, and 121, for cell 102, system backplane 118, and PCI backplane 125, respectively.

[0027] At step 315, state machine 103 monitors the management processor OK signal 108 to determine whether management processor 105 is again operational. When it is determined that management processor 105 is operational, control is passed to the

management processor, and high-availability controller 101 resumes its status monitoring function at step 300.

#### High-Availability Controller Logic

**[0028]** Figure 4 is a block diagram illustrating, in greater detail, the high-availability controller of the present system. As shown in Figure 4, high-availability controller (HAC) 101 centralizes control and status information for access by the management processor 105. In an exemplary embodiment of the present system, high-availability controller 101 is implemented as a Field Programmable Gate Array (FPGA), although other non-software coded devices could, alternatively, be employed. In any event, HAC 101 does not perform the same sequence of operations as the code executed by management processor 105.

**[0029]** The following sensor and control signals are either received or generated by the HAC while monitoring the operation of system 100:

- (1) Front panel power switch 110 is monitored by high-availability controller 101.
- (2) Fan fault signals report fan problems detected by fan module 140. Fan faults, as well as backplane power faults, are reported via interrupt bus 401, except for cell boards 102, from which fan fault signals are sent to the corresponding local service processor 116).
- (3) A 'device present' signal 405 is sent from each major board, i.e., cell 102, PCI 125, and core IO/management processor 104 (as well as front panel & mass storage boards [not shown]) in the system indicating that the board has been properly inserted into the system.
- (4) 'Power Enable' signals 420 are sent to each LPM 15x to control the power of each associated powerable entity. 'Power good' status, via signals 410 from the main power supplies and the powerable entities, confirms proper power up and power down for each entity.
- (5) An 'LPM Ready' signal 415 comes from each board in the system. This signal indicates that the specific LPM 15x has been properly reset, all necessary resources are present, and the LPM is ready to power up the associated board.
- (6) Front panel indicators (LEDs or other display devices) 130 of main power, standby power, management processor OK, and other indicators controlled by the operating system, are controllable by high-availability controller 101.

**[0030]** The buses indicated by lines 402 and 403 are internal to the high-availability controller FPGA, and function as 'data out' and 'data in' lines, respectively. In an exemplary

embodiment of the present system, block 106 is an I2C bus interface that provides a remote interface between management processor 105 and the sensors and controls described above.

#### High-availability Controller Operation State Machine

[0031] Figure 5 is a flowchart showing an exemplary sequence of steps performed by the high-availability controller operation state machine 103. As shown in Figure 5, after a system boot operation at step 505, wherein all management processors 105(1) – 105(N) initiate execution of their respective operating systems, at step 510, the management processor 105 that has been designated as the default primary management processor 105(P) notifies high-availability controller 101 of its primary processor status. High-availability controller 101 then enables management processor 105(P) so that it controls all system functions for which the management processor is responsible, including the monitoring and control functions described above, via I2C bus 111. All management processors 105 receive inputs from power, fan, and temperature sensors 120 (via I2C bus 111), but only primary management processor 105(P) controls the related system functions.

[0032] At step 515, all management processors 105 (1) – 105(N) start (reset) their watchdog timers 117. In the present exemplary embodiment, each watchdog timer 117 has a user-adjustable timeout period of between approximately 6 and 10 seconds, but other timer values may be selected, as appropriate for a particular system 100. At step 520, management processor OK (MP\_OK) signal 108, which is held in an active state as long as watchdog timer 117 is running, is sent to high-availability controller 101. When a given management processor 105 is functioning properly, it periodically sends a reset signal to watchdog timer 117 to cause the timer to restart the timeout period. If a particular management processor 105 malfunctions, it is likely that the processor will not reset the watchdog timer, which will then time out, causing the MP\_OK signal 108 to go inactive. When high-availability controller 101 detects an inactive MP\_OK signal, the controller takes over control of system 100, as described with respect to step 310 in Figure 3, above.

[0033] At step 525, if a watchdog timer reset signal has been sent from primary management processor 105(P), then the timer is reset, at step 515. Otherwise, at step 530, management processor 105(P) checks the status of the system environment. Management processor 105 includes a firmware task that compares system power, temperature, and fan speed with predetermined values to check the integrity of the system operating environment. If the system environmental parameters are not within an acceptable range, then management processor 105(P) does not reset the watchdog timer 117, which causes MP\_OK signal 108 to

go inactive, at step 540. High-availability controller 101 then takes over control of system 100, as described above. If the system environmental parameters are within an acceptable range, then at step 535, if watchdog timer 117 has not timed out, management processor loops back to step 525.

**[0034]** While exemplary embodiments of the present invention have been shown in the drawings and described above, it will be apparent to one skilled in the art that various embodiments of the present invention are possible. For example, the specific configuration of the system as shown in Figures 1, 2, and 4, as well as the particular sequence of steps described above in Figures 3 and 5, should not be construed as limited to the specific embodiments described herein. Modification may be made to these and other specific elements of the invention without departing from its spirit and scope as expressed in the following claims.

FIG. 1  
FIG. 2  
FIG. 3  
FIG. 4  
FIG. 5  
FIG. 6  
FIG. 7  
FIG. 8  
FIG. 9  
FIG. 10  
FIG. 11  
FIG. 12  
FIG. 13  
FIG. 14  
FIG. 15  
FIG. 16  
FIG. 17  
FIG. 18  
FIG. 19  
FIG. 20  
FIG. 21  
FIG. 22  
FIG. 23  
FIG. 24  
FIG. 25  
FIG. 26  
FIG. 27  
FIG. 28  
FIG. 29  
FIG. 30  
FIG. 31  
FIG. 32  
FIG. 33  
FIG. 34  
FIG. 35  
FIG. 36  
FIG. 37  
FIG. 38  
FIG. 39  
FIG. 40  
FIG. 41  
FIG. 42  
FIG. 43  
FIG. 44  
FIG. 45  
FIG. 46  
FIG. 47  
FIG. 48  
FIG. 49  
FIG. 50  
FIG. 51  
FIG. 52  
FIG. 53  
FIG. 54  
FIG. 55  
FIG. 56  
FIG. 57  
FIG. 58  
FIG. 59  
FIG. 60  
FIG. 61  
FIG. 62  
FIG. 63  
FIG. 64  
FIG. 65  
FIG. 66  
FIG. 67  
FIG. 68  
FIG. 69  
FIG. 70  
FIG. 71  
FIG. 72  
FIG. 73  
FIG. 74  
FIG. 75  
FIG. 76  
FIG. 77  
FIG. 78  
FIG. 79  
FIG. 80  
FIG. 81  
FIG. 82  
FIG. 83  
FIG. 84  
FIG. 85  
FIG. 86  
FIG. 87  
FIG. 88  
FIG. 89  
FIG. 90  
FIG. 91  
FIG. 92  
FIG. 93  
FIG. 94  
FIG. 95  
FIG. 96  
FIG. 97  
FIG. 98  
FIG. 99  
FIG. 100  
FIG. 101  
FIG. 102  
FIG. 103  
FIG. 104  
FIG. 105  
FIG. 106  
FIG. 107  
FIG. 108  
FIG. 109  
FIG. 110  
FIG. 111  
FIG. 112  
FIG. 113  
FIG. 114  
FIG. 115  
FIG. 116  
FIG. 117  
FIG. 118  
FIG. 119  
FIG. 120  
FIG. 121  
FIG. 122  
FIG. 123  
FIG. 124  
FIG. 125  
FIG. 126  
FIG. 127  
FIG. 128  
FIG. 129  
FIG. 130  
FIG. 131  
FIG. 132  
FIG. 133  
FIG. 134  
FIG. 135  
FIG. 136  
FIG. 137  
FIG. 138  
FIG. 139  
FIG. 140  
FIG. 141  
FIG. 142  
FIG. 143  
FIG. 144  
FIG. 145  
FIG. 146  
FIG. 147  
FIG. 148  
FIG. 149  
FIG. 150  
FIG. 151  
FIG. 152  
FIG. 153  
FIG. 154  
FIG. 155  
FIG. 156  
FIG. 157  
FIG. 158  
FIG. 159  
FIG. 160  
FIG. 161  
FIG. 162  
FIG. 163  
FIG. 164  
FIG. 165  
FIG. 166  
FIG. 167  
FIG. 168  
FIG. 169  
FIG. 170  
FIG. 171  
FIG. 172  
FIG. 173  
FIG. 174  
FIG. 175  
FIG. 176  
FIG. 177  
FIG. 178  
FIG. 179  
FIG. 180  
FIG. 181  
FIG. 182  
FIG. 183  
FIG. 184  
FIG. 185  
FIG. 186  
FIG. 187  
FIG. 188  
FIG. 189  
FIG. 190  
FIG. 191  
FIG. 192  
FIG. 193  
FIG. 194  
FIG. 195  
FIG. 196  
FIG. 197  
FIG. 198  
FIG. 199  
FIG. 200  
FIG. 201  
FIG. 202  
FIG. 203  
FIG. 204  
FIG. 205  
FIG. 206  
FIG. 207  
FIG. 208  
FIG. 209  
FIG. 210  
FIG. 211  
FIG. 212  
FIG. 213  
FIG. 214  
FIG. 215  
FIG. 216  
FIG. 217  
FIG. 218  
FIG. 219  
FIG. 220  
FIG. 221  
FIG. 222  
FIG. 223  
FIG. 224  
FIG. 225  
FIG. 226  
FIG. 227  
FIG. 228  
FIG. 229  
FIG. 230  
FIG. 231  
FIG. 232  
FIG. 233  
FIG. 234  
FIG. 235  
FIG. 236  
FIG. 237  
FIG. 238  
FIG. 239  
FIG. 240  
FIG. 241  
FIG. 242  
FIG. 243  
FIG. 244  
FIG. 245  
FIG. 246  
FIG. 247  
FIG. 248  
FIG. 249  
FIG. 250  
FIG. 251  
FIG. 252  
FIG. 253  
FIG. 254  
FIG. 255  
FIG. 256  
FIG. 257  
FIG. 258  
FIG. 259  
FIG. 260  
FIG. 261  
FIG. 262  
FIG. 263  
FIG. 264  
FIG. 265  
FIG. 266  
FIG. 267  
FIG. 268  
FIG. 269  
FIG. 270  
FIG. 271  
FIG. 272  
FIG. 273  
FIG. 274  
FIG. 275  
FIG. 276  
FIG. 277  
FIG. 278  
FIG. 279  
FIG. 280  
FIG. 281  
FIG. 282  
FIG. 283  
FIG. 284  
FIG. 285  
FIG. 286  
FIG. 287  
FIG. 288  
FIG. 289  
FIG. 290  
FIG. 291  
FIG. 292  
FIG. 293  
FIG. 294  
FIG. 295  
FIG. 296  
FIG. 297  
FIG. 298  
FIG. 299  
FIG. 300  
FIG. 301  
FIG. 302  
FIG. 303  
FIG. 304  
FIG. 305  
FIG. 306  
FIG. 307  
FIG. 308  
FIG. 309  
FIG. 310  
FIG. 311  
FIG. 312  
FIG. 313  
FIG. 314  
FIG. 315  
FIG. 316  
FIG. 317  
FIG. 318  
FIG. 319  
FIG. 320  
FIG. 321  
FIG. 322  
FIG. 323  
FIG. 324  
FIG. 325  
FIG. 326  
FIG. 327  
FIG. 328  
FIG. 329  
FIG. 330  
FIG. 331  
FIG. 332  
FIG. 333  
FIG. 334  
FIG. 335  
FIG. 336  
FIG. 337  
FIG. 338  
FIG. 339  
FIG. 340  
FIG. 341  
FIG. 342  
FIG. 343  
FIG. 344  
FIG. 345  
FIG. 346  
FIG. 347  
FIG. 348  
FIG. 349  
FIG. 350  
FIG. 351  
FIG. 352  
FIG. 353  
FIG. 354  
FIG. 355  
FIG. 356  
FIG. 357  
FIG. 358  
FIG. 359  
FIG. 360  
FIG. 361  
FIG. 362  
FIG. 363  
FIG. 364  
FIG. 365  
FIG. 366  
FIG. 367  
FIG. 368  
FIG. 369  
FIG. 370  
FIG. 371  
FIG. 372  
FIG. 373  
FIG. 374  
FIG. 375  
FIG. 376  
FIG. 377  
FIG. 378  
FIG. 379  
FIG. 380  
FIG. 381  
FIG. 382  
FIG. 383  
FIG. 384  
FIG. 385  
FIG. 386  
FIG. 387  
FIG. 388  
FIG. 389  
FIG. 390  
FIG. 391  
FIG. 392  
FIG. 393  
FIG. 394  
FIG. 395  
FIG. 396  
FIG. 397  
FIG. 398  
FIG. 399  
FIG. 400  
FIG. 401  
FIG. 402  
FIG. 403  
FIG. 404  
FIG. 405  
FIG. 406  
FIG. 407  
FIG. 408  
FIG. 409  
FIG. 410  
FIG. 411  
FIG. 412  
FIG. 413  
FIG. 414  
FIG. 415  
FIG. 416  
FIG. 417  
FIG. 418  
FIG. 419  
FIG. 420  
FIG. 421  
FIG. 422  
FIG. 423  
FIG. 424  
FIG. 425  
FIG. 426  
FIG. 427  
FIG. 428  
FIG. 429  
FIG. 430  
FIG. 431  
FIG. 432  
FIG. 433  
FIG. 434  
FIG. 435  
FIG. 436  
FIG. 437  
FIG. 438  
FIG. 439  
FIG. 440  
FIG. 441  
FIG. 442  
FIG. 443  
FIG. 444  
FIG. 445  
FIG. 446  
FIG. 447  
FIG. 448  
FIG. 449  
FIG. 450  
FIG. 451  
FIG. 452  
FIG. 453  
FIG. 454  
FIG. 455  
FIG. 456  
FIG. 457  
FIG. 458  
FIG. 459  
FIG. 460  
FIG. 461  
FIG. 462  
FIG. 463  
FIG. 464  
FIG. 465  
FIG. 466  
FIG. 467  
FIG. 468  
FIG. 469  
FIG. 470  
FIG. 471  
FIG. 472  
FIG. 473  
FIG. 474  
FIG. 475  
FIG. 476  
FIG. 477  
FIG. 478  
FIG. 479  
FIG. 480  
FIG. 481  
FIG. 482  
FIG. 483  
FIG. 484  
FIG. 485  
FIG. 486  
FIG. 487  
FIG. 488  
FIG. 489  
FIG. 490  
FIG. 491  
FIG. 492  
FIG. 493  
FIG. 494  
FIG. 495  
FIG. 496  
FIG. 497  
FIG. 498  
FIG. 499  
FIG. 500  
FIG. 501  
FIG. 502  
FIG. 503  
FIG. 504  
FIG. 505  
FIG. 506  
FIG. 507  
FIG. 508  
FIG. 509  
FIG. 510  
FIG. 511  
FIG. 512  
FIG. 513  
FIG. 514  
FIG. 515  
FIG. 516  
FIG. 517  
FIG. 518  
FIG. 519  
FIG. 520  
FIG. 521  
FIG. 522  
FIG. 523  
FIG. 524  
FIG. 525  
FIG. 526  
FIG. 527  
FIG. 528  
FIG. 529  
FIG. 530  
FIG. 531  
FIG. 532  
FIG. 533  
FIG. 534  
FIG. 535  
FIG. 536  
FIG. 537  
FIG. 538  
FIG. 539  
FIG. 540  
FIG. 541  
FIG. 542  
FIG. 543  
FIG. 544  
FIG. 545  
FIG. 546  
FIG. 547  
FIG. 548  
FIG. 549  
FIG. 550  
FIG. 551  
FIG. 552  
FIG. 553  
FIG. 554  
FIG. 555  
FIG. 556  
FIG. 557  
FIG. 558  
FIG. 559  
FIG. 560  
FIG. 561  
FIG. 562  
FIG. 563  
FIG. 564  
FIG. 565  
FIG. 566  
FIG. 567  
FIG. 568  
FIG. 569  
FIG. 570  
FIG. 571  
FIG. 572  
FIG. 573  
FIG. 574  
FIG. 575  
FIG. 576  
FIG. 577  
FIG. 578  
FIG. 579  
FIG. 580  
FIG. 581  
FIG. 582  
FIG. 583  
FIG. 584  
FIG. 585  
FIG. 586  
FIG. 587  
FIG. 588  
FIG. 589  
FIG. 590  
FIG. 591  
FIG. 592  
FIG. 593  
FIG. 594  
FIG. 595  
FIG. 596  
FIG. 597  
FIG. 598  
FIG. 599  
FIG. 600  
FIG. 601  
FIG. 602  
FIG. 603  
FIG. 604  
FIG. 605  
FIG. 606  
FIG. 607  
FIG. 608  
FIG. 609  
FIG. 610  
FIG. 611  
FIG. 612  
FIG. 613  
FIG. 614  
FIG. 615  
FIG. 616  
FIG. 617  
FIG. 618  
FIG. 619  
FIG. 620  
FIG. 621  
FIG. 622  
FIG. 623  
FIG. 624  
FIG. 625  
FIG. 626  
FIG. 627  
FIG. 628  
FIG. 629  
FIG. 630  
FIG. 631  
FIG. 632  
FIG. 633  
FIG. 634  
FIG. 635  
FIG. 636  
FIG. 637  
FIG. 638  
FIG. 639  
FIG. 640  
FIG. 641  
FIG. 642  
FIG. 643  
FIG. 644  
FIG. 645  
FIG. 646  
FIG. 647  
FIG. 648  
FIG. 649  
FIG. 650  
FIG. 651  
FIG. 652  
FIG. 653  
FIG. 654  
FIG. 655  
FIG. 656  
FIG. 657  
FIG. 658  
FIG. 659  
FIG. 660  
FIG. 661  
FIG. 662  
FIG. 663  
FIG. 664  
FIG. 665  
FIG. 666  
FIG. 667  
FIG. 668  
FIG. 669  
FIG. 670  
FIG. 671  
FIG. 672  
FIG. 673  
FIG. 674  
FIG. 675  
FIG. 676  
FIG. 677  
FIG. 678  
FIG. 679  
FIG. 680  
FIG. 681  
FIG. 682  
FIG. 683  
FIG. 684  
FIG. 685  
FIG. 686  
FIG. 687  
FIG. 688  
FIG. 689  
FIG. 690  
FIG. 691  
FIG. 692  
FIG. 693  
FIG. 694  
FIG. 695  
FIG. 696  
FIG. 697  
FIG. 698  
FIG. 699  
FIG. 700  
FIG. 701  
FIG. 702  
FIG. 703  
FIG. 704  
FIG. 705  
FIG. 706  
FIG. 707  
FIG. 708  
FIG. 709  
FIG. 710  
FIG. 711  
FIG. 712  
FIG. 713  
FIG. 714  
FIG. 715  
FIG. 716  
FIG. 717  
FIG. 718  
FIG. 719  
FIG. 720  
FIG. 721  
FIG. 722  
FIG. 723  
FIG. 724  
FIG. 725  
FIG. 726  
FIG. 727  
FIG. 728  
FIG. 729  
FIG. 730  
FIG. 731  
FIG. 732  
FIG. 733  
FIG. 734  
FIG. 735  
FIG. 736  
FIG. 737  
FIG. 738  
FIG. 739  
FIG. 740  
FIG. 741  
FIG. 742  
FIG. 743  
FIG. 744  
FIG. 745  
FIG. 746  
FIG. 747  
FIG. 748  
FIG. 749  
FIG. 750  
FIG. 751  
FIG. 752  
FIG. 753  
FIG. 754  
FIG. 755  
FIG. 756  
FIG. 757  
FIG. 758  
FIG. 759  
FIG. 760  
FIG. 761  
FIG. 762  
FIG. 763  
FIG. 764  
FIG. 765  
FIG. 766  
FIG. 767  
FIG. 768  
FIG. 769  
FIG. 770  
FIG. 771  
FIG. 772  
FIG. 773  
FIG. 774  
FIG. 775  
FIG. 776  
FIG. 777  
FIG. 778  
FIG. 779  
FIG. 780  
FIG. 781  
FIG. 782  
FIG. 783  
FIG. 784  
FIG. 785  
FIG. 786  
FIG. 787  
FIG. 788  
FIG. 789  
FIG. 790  
FIG. 791  
FIG. 792  
FIG. 793  
FIG. 794  
FIG. 795  
FIG. 796  
FIG. 797  
FIG. 798  
FIG. 799  
FIG. 800  
FIG. 801  
FIG. 802  
FIG. 803  
FIG. 804  
FIG. 805  
FIG. 806  
FIG. 807  
FIG. 808  
FIG. 809  
FIG. 810  
FIG. 811  
FIG. 812  
FIG. 813  
FIG. 814  
FIG. 815  
FIG. 816  
FIG. 817  
FIG. 818  
FIG. 819  
FIG. 820  
FIG. 821  
FIG. 822  
FIG. 823  
FIG. 824  
FIG. 825  
FIG. 826  
FIG. 827  
FIG. 828  
FIG. 829  
FIG. 830  
FIG. 831  
FIG. 832  
FIG. 833  
FIG. 834  
FIG. 835  
FIG. 836  
FIG. 837  
FIG. 838  
FIG. 839  
FIG. 840  
FIG. 841  
FIG. 842  
FIG. 843  
FIG. 844  
FIG. 845  
FIG. 846  
FIG. 847  
FIG. 848  
FIG. 849  
FIG. 850  
FIG. 851  
FIG. 852  
FIG. 853  
FIG. 854  
FIG. 855  
FIG. 856  
FIG. 857  
FIG. 858  
FIG. 859  
FIG. 860  
FIG. 861  
FIG. 862  
FIG. 863  
FIG. 864  
FIG. 865  
FIG. 866  
FIG. 867  
FIG. 868  
FIG. 869  
FIG. 870  
FIG. 871  
FIG. 872  
FIG. 873  
FIG. 874  
FIG. 875  
FIG. 876  
FIG. 877  
FIG. 878  
FIG. 879  
FIG. 880  
FIG. 881  
FIG. 882  
FIG. 883  
FIG. 884  
FIG. 885  
FIG. 886  
FIG. 887  
FIG. 888  
FIG. 889  
FIG. 890  
FIG. 891  
FIG. 892  
FIG. 893  
FIG. 894  
FIG. 895  
FIG. 896  
FIG. 897  
FIG. 898  
FIG. 899  
FIG. 900  
FIG. 901  
FIG. 902  
FIG. 903  
FIG. 904  
FIG. 905  
FIG. 906  
FIG. 907  
FIG. 908  
FIG. 909  
FIG. 910  
FIG. 911  
FIG. 912  
FIG. 913  
FIG. 914  
FIG. 915  
FIG. 916  
FIG. 917  
FIG. 918  
FIG. 919  
FIG. 920  
FIG. 921  
FIG. 922  
FIG. 923  
FIG. 924  
FIG. 925  
FIG. 926  
FIG. 927  
FIG. 928  
FIG. 929  
FIG. 930  
FIG. 931  
FIG. 932  
FIG. 933  
FIG. 934  
FIG. 935  
FIG. 936  
FIG. 937  
FIG. 938  
FIG. 939  
FIG. 940  
FIG. 941  
FIG. 942  
FIG. 943  
FIG. 944  
FIG. 945  
FIG. 946  
FIG. 947  
FIG. 948  
FIG. 949  
FIG. 950  
FIG. 951  
FIG. 952  
FIG. 953  
FIG. 954  
FIG. 955  
FIG. 956  
FIG. 957  
FIG. 958  
FIG. 959  
FIG. 960  
FIG. 961  
FIG. 962  
FIG. 963  
FIG. 964  
FIG. 965  
FIG. 966  
FIG. 967  
FIG. 968  
FIG. 969  
FIG. 970  
FIG. 971  
FIG. 972  
FIG. 973  
FIG. 974  
FIG. 975  
FIG. 976  
FIG. 977  
FIG. 978  
FIG. 979  
FIG. 980  
FIG. 981  
FIG. 982  
FIG. 983  
FIG. 984  
FIG. 985  
FIG. 986  
FIG. 987  
FIG. 988  
FIG. 989  
FIG. 990  
FIG. 991  
FIG. 992  
FIG. 993  
FIG. 994  
FIG. 995  
FIG. 996  
FIG. 997  
FIG. 998  
FIG. 999  
FIG. 1000